

कार्यालय प्राचार्य, शासकीय पॉलीटेक्निक जशपुर (छ.ग.)

ग्राम-झरगॉव, पोस्ट- घोलेंग, तह. जशपुर, जिला- जशपुर (छ.ग.) पिन कोड -496338

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LESSON PLAN SESSION Jan.-June 2024-25

SUBJECT: **Computer Organisation & Microprocessor (COM)**

SEMESTER: **4th**

BRANCH: - **Computer Science Engineering**

UNIT NUMBER	NAME OF THE TOPIC	NO OF CLASS REQUIRED	REMARK
Unit 1.0 8085 Microprocessor	1.1 List of terms used in Microprocessor. 1.1.1 Instruction Set 1.1.2 Clock Speed 1.1.3 Bandwidth 1.1.4 Bandwidth 1.1.5 Word Length 1.1.6 Data Types	01	
	1.2 Features of Microprocessor	01	
	1.3 8085 Architecture and block diagram	02	
	1.4 8085 Functional units 1.2.1 Multiplexed address/ data Bus 1.2.2 Accumulator 1.2.3 Arithmetic and Logic Unit 1.2.4 General Purpose Registers 1.2.5 Program Counter 1.2.6 Stack Pointer 1.2.7 Flag Register	01	
	1.5 8085 Pin Configuration	01	
	<ul style="list-style-type: none">Concepts beyond class	01	
	<ul style="list-style-type: none">QUIZ.Doubt clearing session	01	ASSIGNMENT-1
Unit 2.0 Addressing Modes & Instruction set of 8085	2.1 Instruction cycle 2.1.1 Opcode fetch cycle 2.1.2 Execution cycle	01	
	2.2 Timing Diagram 2.2.1 Opcode fetch 2.2.2 Memory Read 2.2.3 Memory Write 2.2.4 MOV R1, R2 2.2.5 MOV R, Mem 2.2.6 MOV Mem, R	02	
	2.2 Addressing modes in 8085 2.2.1 Immediate Addressing Mode 2.2.2 Register Addressing Mode 2.2.3 Direct Addressing Modes 2.2.4 Indirect addressing Mode	01	
	2.2 2.5 Instruction set of 8085 2.2.1 Data Movement Instructions 2.2.2 Arithmetic instructions 2.2.3 Logical Instructions 2.2.4 Shift & Rotate instructions 2.2.5 Program Control instructions 2.2.6 Branching instructions Stack instructions	02	
	<ul style="list-style-type: none">Concepts beyond class	01	
	<ul style="list-style-type: none">QUIZDoubt clearing session	01	ASSIGNMENT-2
Unit 3.0 Assembly Language Programming for 8085	3.1 Machine Language, Assembly language,	01	
	3.2 Assemblers first pass, Second Pass	02	
	3.3 Assembly language programming 3.3.1 Arithmetic operation of two numbers (both numbers stored in R, Mem& Immediate)	02	

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	3.3.2 Swapping of two numbers stored in registers & memory Program for Stack using PUSH, POP		
	3.4 8085 Interrupt Structure 3.4.1 Hardware Interrupts 3.4.2. Software Interrupts	02	
	3.5 Architectural block diagram of 8086	01	
	<ul style="list-style-type: none"> Concepts beyond class 	01	
	<ul style="list-style-type: none"> QUIZ Doubt clearing session 	01	ASSIGNMENT-3
Unit 4.0 Input Output Organization	4.1 Input Output Interface I/O Bus and Interface 4.1.2 I/O vs. Memory Bus 4.1.3 Isolated vs. Memory Mapped I/O	01	
	4.2 Asynchronous Data Transfer 4.2.1 Strobe Control 4.2.2 Handshaking	02	
	4.3 Modes of Transfer 4.3.1 Programmed I/O 4.3.2 Interrupt initiated I/O 4.3.3 Software considerations	02	
	4.4 Direct Memory Access 4.4.1 DMA Controller 4.4.2 DMA Transfer	02	
	4.5 Input Output Processor 4.5.1 CPU-IOP Communication	01	
	<ul style="list-style-type: none"> Concepts beyond class 	01	
	<ul style="list-style-type: none"> QUIZ Doubt clearing session 	01	ASSIGNMENT-4
Unit 5.0 Memory Organization	5.1 Memory hierarchy	01	
	5.2 Auxiliary Memory 5.2.1 Magnetic Disks 5.2.2 Magnetic Tape	02	
	5.3 Cache Memory 5.3.1 Associative Mapping 5.3.2 Direct Mapping 5.3.3 Set Associative Mapping 5.3.4 Virtual Memory	02	
	5.4.1 Address Space and Memory Space 5.4.2 Address Mapping using Pages 5.4.3 Associative Memory Page table	02	
	5.5 Memory Management Hardware	01	
	<ul style="list-style-type: none"> Concepts beyond class 	01	
	<ul style="list-style-type: none"> QUIZ Doubt clearing session 	01	ASSIGNMENT-5
Total Classes Required		48	

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LECTURER, ET&T, GPJ

HOD CSE Sign: -

